1. General:

- The HC210M-R is a low-cost sub-1 GHz receiver designed for very low-power wireless applications. The circuit is mainly intended for the ISM (Industrial, Scientific and Medical) and SRD (Short Range Device) frequency bands at 315, 433, 868, and 915 MHz, but can easily be programmed for operation at other frequencies in the 300-348 MHz, 387-464 MHz and 779-928 MHz bands.
- Suited for systems targeting compliance with EN 300 220 (Europe) and FCC CFR Part 15(US).
- Suited for systems targeting compliance with the Wireless MBUS standard EN 13757-4:2005
- Support for asynchronous and synchronous serial receive/transmit mode for backwards compatibility with existing radio communication protocols

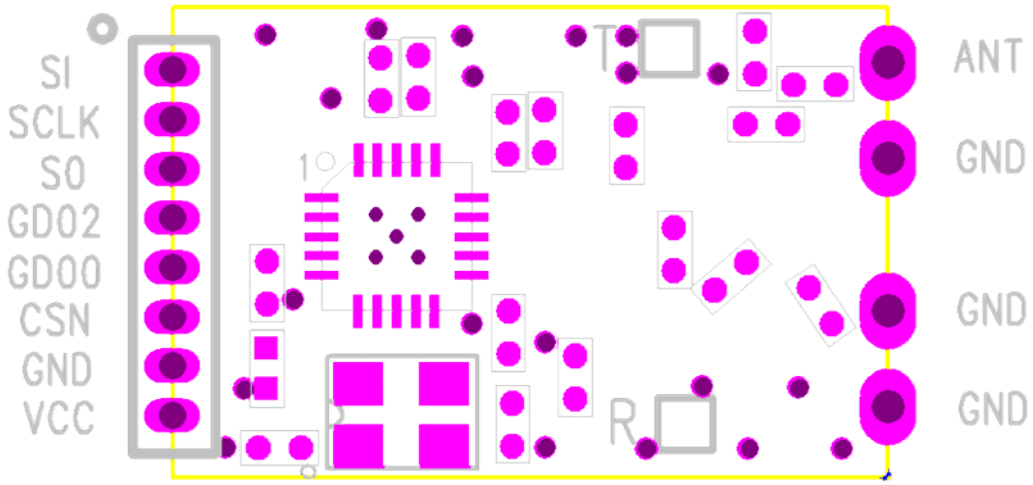
2. Applications：

- Ultra low-power wireless applications operating in the 315/433/868/915 MHz ISM/SRD bands
- Wireless alarm and security systems
- Industrial monitoring and control
- Wireless sensor networks
- AMR – Automatic Meter Reading
- Home and building automation
- Wireless MBUS

3. Features：

- High sensitivity
  - -116 dBm at 0.6 kBaud, 433 MHz,1% packet error rate
  - -112 dBm at 1.2 kBaud, 868 MHz,1% packet error rate
- Low current consumption (14.7 mA in RX,1.2 kBaud, 868 MHz)
- Programmable output power up to +12 dBm for all supported frequencies
- Excellent receiver selectivity and blocking performance
- Programmable data rate from 0.6 to 600 kbps
- Frequency bands: 300-348 MHz, 387-464MHz and 779-928 MHz
- 2-FSK, 4-FSK, GFSK, and MSK supported as well as OOK and flexible ASK shaping
- Suitable for frequency hopping systems due to a fast settling frequency synthesizer; 75 µs settling time
- Automatic Frequency Compensation (AFC) can be used to align the frequency synthesizer to the received signal centre frequency
- Integrated analog temperature sensor
- Flexible support for packet oriented systems; On-chip support for sync word detection, address check, flexible packet length, and automatic CRC handling
- Efficient SPI interface; All registers can be programmed with one “burst” transfer
- Digital RSSI output
- Programmable channel filter bandwidth
- Programmable Carrier Sense (CS) indicator
- Programmable Preamble Quality Indicator (PQI) for improved protection against false sync word detection in random noise
- Support for automatic Clear Channel Assessment (CCA) before transmitting (for listen-before-talk systems)
- Support for per-package Link Quality Indication (LQI)
- Optional automatic whitening and de- whitening of data
- 200 nA sleep mode current consumption
- Fast startup time; 240 µs from sleep to RX or TX mode (measured on EM reference design [2] and[3])
- Wake-on-radio functionality for automatic low-power RX polling
- Separate 64-byte RX and TX data FIFOs(enables burst mode data transmission)

4. PIN Description



Pin #	Pin Name	Pin type	Description
1	SI	Digital Input	Serial configuration interface, data input
2	SCLK	Digital Input	Serial configuration interface, clock input
3	SO(GDO1)	Digital Output	Serial configuration interface, data output Optional general output pin when CSn is high
4	GDO02	Digital Output	Digital output pin for general use: • Test signals • FIFO status signals • Clock output, down-divided from XOSC • Serial output RX data
5	GDO0	Digital Output	Digital output pin for general use: • Test signals • FIFO status signals • Clock output, down-divided from XOSC • Serial output RX data
6	SCN	Digital Input	Serial configuration interface, chip select.
7	GND	Ground	Module ground.
8	VDD	Power supply+	1.8-3.6V power supply for module
9	ANT	Digital Input	Module Antenna terminal, Default terminal
10,11,12	GND	Ground	Module ground.

5. Absolute Maximum Ratings

Under no circumstances must the absolute maximum ratings given in Table 1 be violated. Stress

exceeding one or more of the limiting values may cause permanent damage to the device.

Parameter	Min	Max	Units	Condition
Supply voltage	–0.3	3.9	V	All supply pins must have the same voltage
Voltage on any digital pin	–0.3	VDD + 0.3, max 3.9	V	
Voltage on the pins RF_P, RF_N, DCOUPL, RBIAS	–0.3	2.0	V	
Voltage ramp-up rate		120	kV/µs	
Input RF level		+10	dBm	
Storage temperature range	–50	150	°C	
Solder reflow temperature		260	°C	According to IPC/JEDEC J-STD-020
ESD		750	V	According to JEDEC STD 22, method A114, Human Body Model (HBM)
ESD		400	V	According to JEDEC STD 22, C101C, Charged Device Model (CDM)

Table 1: Absolute Maximum Ratings

Caution! *ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.*

6. Operating Conditions

The operating conditions for **HC210M-R** are listed Table 2 in below.

Parameter	Min	Max	Unit	Condition
Operating temperature	-40	85	°C	
Operating supply voltage	1.8	3.6	V	All supply pins must have the same voltage

Table 2: Operating Conditions

7. General Characteristics

Parameter	Min	Typ	Max	Unit	Condition/Note
Frequency range	300		348	MHz	
	387		464	MHz	If using a 27 MHz crystal, the lower frequency limit for this band is 392 MHz
	779		928	MHz	
Data rate	0.6		500	kBaud	2-FSK
	0.6		250	kBaud	GFSK, OOK, and ASK
	0.6		300	kBaud	4-FSK (the data rate in kbps will be twice the baud rate)
	26		500	kBaud	(Shaped) MSK (also known as differential offset QPSK).
					Optional Manchester encoding (the data rate in kbps will be half the baud rate)

Table 3: General Characteristics

8. Electrical Specifications

8.1 Current Consumption

T_A = 25°C, VDD = 3.0 V if nothing else stated. All measurement results are obtained using the CC113EM reference designs ([2] and [3]). Reduced current settings (`MDMCFG2.DEM_DCFILT_OFF=1`) gives a slightly lower current consumption at the cost of a reduction in sensitivity. See Table 7 for additional details on current consumption and sensitivity.

Parameter	Min	Typ	Max	Unit	Condition
Current consumption in power down modes		0.2	1	µA	Voltage regulator to digital part off, register values retained (SLEEP state). All GDO pins programmed to 0x2F (HW to 0)
		0.5		µA	Voltage regulator to digital part off, register values retained, low-power RC oscillator running (SLEEP state with WOR enabled)
		100		µA	Voltage regulator to digital part off, register values retained, XOSC running (SLEEP state with `MCSM0.OSC_FORCE_ON` set)
		165		µA	Voltage regulator to digital part on, all other modules in power down (XOFF state)
Current consumption		8.8		µA	Automatic RX polling once each second, using low-power RC oscillator, with 542 kHz filter bandwidth and 250 kBaud data rate, PLL calibration every 4th wakeup. Average current with signal in channel *below* carrier sense level (`MCSM2.RX_TIME_RSSI=1`)
		35.3		µA	Same as above, but with signal in channel *above* carrier sense level, 1.96 ms RX timeout, and no preamble/sync word found
		1.4		µA	Automatic RX polling every 15th second, using low-power RC oscillator, with 542 kHz filter bandwidth and 250 kBaud data rate, PLL calibration every 4th wakeup. Average current with signal in channel below carrier sense level (`MCSM2.RX_TIME_RSSI=1`)
		39.3		µA	Same as above, but with signal in channel *above* carrier sense level, 36.6 ms RX timeout, and no preamble/sync word found
		1.7		mA	Only voltage regulator to digital part and crystal oscillator running (IDLE state)
		8.4		mA	Only the frequency synthesizer is running (FSTXON state). This currents consumption is also representative for the other intermediate states when going from IDLE to RX or TX, including the calibration state
Current consumption, 315 MHz		15.4		mA	Receive mode, 1.2 kBaud, reduced current, input at sensitivity limit
		14.4		mA	Receive mode, 1.2 kBaud, register settings optimized for reduced current, input well above sensitivity limit
		15.2		mA	Receive mode, 38.4 kBaud, register settings optimized for reduced current, input at sensitivity limit
		14.3		mA	Receive mode, 38.4 kBaud, register settings optimized for reduced current, input well above sensitivity limit
		16.5		mA	Receive mode, 250 kBaud, register settings optimized for reduced current, input at sensitivity limit
		15.1		mA	Receive mode, 250 kBaud, register settings optimized for reduced current, input well above sensitivity limit
		27.4		mA	Transmit mode, +10 dBm output power
		15.0		mA	Transmit mode, 0 dBm output power
		12.3		mA	Transmit mode, –6 dBm output power

Parameter	Min	Typ	Max	Unit	Condition
Current consumption, 433 MHz		16.0		mA	Receive mode, 1.2 kBaud, register settings optimized for reduced current, input at sensitivity limit
		15.0		mA	Receive mode, 1.2 kBaud, register settings optimized for reduced current, input well above sensitivity limit
		15.7		mA	Receive mode, 38.4 kBaud, register settings optimized for reduced current, input at sensitivity limit
		15.0		mA	Receive mode, 38.4 kBaud, register settings optimized for reduced current, input well above sensitivity limit
		17.1		mA	Receive mode, 250 kBaud, register settings optimized for reduced current, input at sensitivity limit
		15.7		mA	Receive mode, 250 kBaud, register settings optimized for reduced current, input well above sensitivity limit
		29.2		mA	Transmit mode, +10 dBm output power
		16.0		mA	Transmit mode, 0 dBm output power
		13.1		mA	Transmit mode, –6 dBm output power
Current consumption, 868/915 MHz		15.7		mA	Receive mode, 1.2 kBaud, register settings optimized for reduced current, input at sensitivity limit. See Figure 1 for current consumption with register settings optimized for sensitivity.
		14.7		mA	Receive mode, 1.2 kBaud, register settings optimized for reduced current, input well above sensitivity limit. See Figure 1 for current consumption with register settings optimized for sensitivity.
		15.6		mA	Receive mode, 38.4 kBaud, register settings optimized for reduced current, input at sensitivity limit. See Figure 1 for current consumption with register settings optimized for sensitivity.
		14.6		mA	Receive mode, 38.4 kBaud, register settings optimized for reduced current, input well above sensitivity limit. See Figure 1 for current consumption with register settings optimized for sensitivity.
		16.9		mA	Receive mode, 250 kBaud, register settings optimized for reduced current, input at sensitivity limit. See Figure 1 for current consumption with register settings optimized for sensitivity.
		15.6		mA	Receive mode, 250 kBaud, register settings optimized for reduced current, input well above sensitivity limit. See Figure 1 for current consumption with register settings optimized for sensitivity.
		34.2		mA	Transmit mode, +12 dBm output power, 868 MHz
		30.0		mA	Transmit mode, +10 dBm output power, 868 MHz
		16.8		mA	Transmit mode, 0 dBm output power, 868 MHz
		16.4		mA	Transmit mode, –6 dBm output power, 868 MHz.
		33.4		mA	Transmit mode, +11 dBm output power, 915 MHz
		30.7		mA	Transmit mode, +10 dBm output power, 915 MHz
		17.2		mA	Transmit mode, 0 dBm output power, 915 MHz
		17.0		mA	Transmit mode, –6 dBm output power, 915 MHz

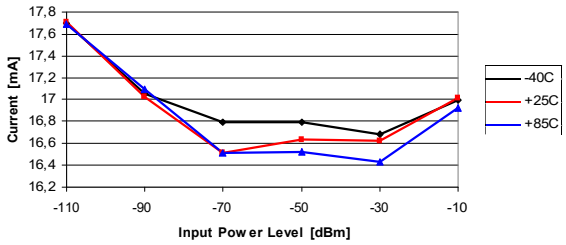
Table 4: Current Consumption

	Supply Voltage VDD = 1.8 V			Supply Voltage VDD = 3.0 V			Supply Voltage VDD = 3.6 V		
Temperature [°C]	-40	25	85	-40	25	85	-40	25	85
Current [mA], PATABLE=0xC0, +12 dBm	32.7	31.5	30.5	35.3	34.2	33.3	35.5	34.4	33.5
Current [mA], PATABLE=0xC5, +10 dBm	30.1	29.2	28.3	30.9	30.0	29.4	31.1	30.3	29.6
Current [mA], PATABLE=0x50, 0 dBm	16.4	16.0	15.6	17.3	16.8	16.4	17.6	17.1	16.7

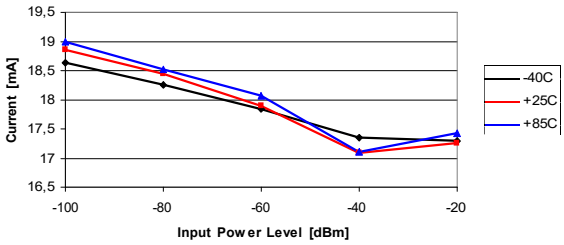
Table 5: Typical TX Current Consumption over Temperature and Supply Voltage, 868 MHz

	Supply Voltage VDD = 1.8 V			Supply Voltage VDD = 3.0 V			Supply Voltage VDD = 3.6 V		
Temperature [°C]	-40	25	85	-40	25	85	-40	25	85
Current [mA], PATABLE=0xC0, +11 dBm	31.9	30.7	29.8	34.6	33.4	32.5	34.8	33.6	32.7
Current [mA], PATABLE=0xC3, +10 dBm	30.9	29.8	28.9	31.7	30.7	30.0	31.9	31.0	30.2
Current [mA], PATABLE=0x8E, 0 dBm	17.2	16.8	16.4	17.6	17.2	16.9	17.8	17.4	17.1

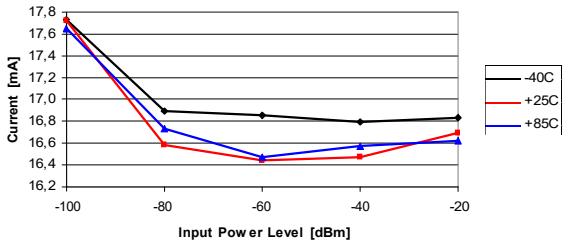
Table 6: Typical TX Current Consumption over Temperature and Supply Voltage, 915 MHz



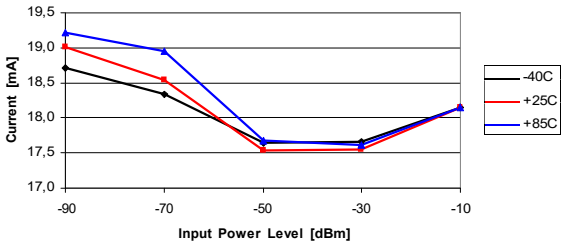
1.2 kBaud GFSK



250 kBaud GFSK



38.4 kBaud GFSK



500 kBaud MSK

Figure 1: Typical RX Current Consumption over Temperature and Input Power Level, 868/915 MHz, Sensitivity Optimized Setting

8.2 RF Receive Section

T_A = 25°C, VDD = 3.0 V if nothing else stated. All measurement results are obtained using the CC113EM reference designs ([2] and [3]).

Parameter	Min	Typ	Max	Unit	Condition/Note
Digital channel filter bandwidth	58		812	kHz	User programmable. The bandwidth limits are proportional to crystal frequency (given values assume a 26.0 MHz crystal)
Spurious emissions		-68	–57	dBm	25 MHz – 1 GHz (Maximum figure is the ETSI EN 300 220 limit)
		-66	–47	dBm	Above 1 GHz (Maximum figure is the ETSI EN 300 220 limit) Typical radiated spurious emission is -49 dBm measured at the VCO frequency
RX latency		9		bit	Serial operation. Time from start of reception until data is available on the receiver data output pin is equal to 9 bit

315 MHz

1.2 kBaud data rate, sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (2-FSK, 1% packet error rate, 20 bytes packet length, 5.2 kHz deviation, 58 kHz digital channel filter bandwidth)					
Receiver sensitivity		-111		dBm	Sensitivity can be traded for current consumption by setting `MDMCFG2.DEM_DCFILT_OFF=1`. The typical current consumption is then reduced from 17.2 mA to 15.4 mA at the sensitivity limit. The sensitivity is typically reduced to -109 dBm
500 kBaud data rate, sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (MSK, 1% packet error rate, 20 bytes packet length, 812 kHz digital channel filter bandwidth)					
Receiver sensitivity		-88		dBm	`MDMCFG2.DEM_DCFILT_OFF`=1 cannot be used for data rates > 250 kBaud

433 MHz

0.6 kBaud data rate, sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (GFSK, 1% packet error rate, 20 bytes packet length, 14.3 kHz deviation, 58 kHz digital channel filter bandwidth)					
Receiver sensitivity		-116		dBm	
1.2 kBaud data rate, sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (GFSK, 1% packet error rate, 20 bytes packet length, 5.2 kHz deviation, 58 kHz digital channel filter bandwidth)					
Receiver sensitivity		-112		dBm	Sensitivity can be traded for current consumption by setting `MDMCFG2.DEM_DCFILT_OFF=1`. The typical current consumption is then reduced from 18.0 mA to 16.0 mA at the sensitivity limit. The sensitivity is typically reduced to -110 dBm
38.4 kBaud data rate, sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (GFSK, 1% packet error rate, 20 bytes packet length, 20 kHz deviation, 100 kHz digital channel filter bandwidth)					
Receiver sensitivity		–104		dBm	
250 kBaud data rate, sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (GFSK, 1% packet error rate, 20 bytes packet length, 127 kHz deviation, 540 kHz digital channel filter bandwidth)					
Receiver sensitivity		-95		dBm	

868/915 MHz

1.2 kBaud data rate, sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (GFSK, 1% packet error rate, 20 bytes packet length, 5.2 kHz deviation, 58 kHz digital channel filter bandwidth)					
Receiver sensitivity		–112		dBm	Sensitivity can be traded for current consumption by setting `MDMCFG2.DEM_DCFILT_OFF=1`. The typical current consumption is then reduced from 17.7 mA to 15.7 mA at sensitivity limit. The sensitivity is typically reduced to -109 dBm
Saturation		–14		dBm	`FIFOTHR.CLOSE_IN_RX=0`. See more in DN010 [11]
Adjacent channel rejection ±100 kHz offset		37		dB	Desired channel 3 dB above the sensitivity limit. 100 kHz channel spacing See Figure 2 for selectivity performance at other offset frequencies
Image channel rejection		31		dB	IF frequency 152 kHz Desired channel 3 dB above the sensitivity limit

Parameter	Min	Typ	Max	Unit	Condition/Note
Blocking ±2 MHz offset ±10 MHz offset		 -50 -40		 dBm dBm	Desired channel 3 dB above the sensitivity limit See Figure 2 for blocking performance at other offset frequencies
38.4 kBaud data rate, sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (GFSK, 1% packet error rate, 20 bytes packet length, 20 kHz deviation, 100 kHz digital channel filter bandwidth)					
Receiver sensitivity		–104		dBm	Sensitivity can be traded for current consumption by setting `MDMCFG2.DEM_DCFILT_OFF=1`. The typical current consumption is then reduced from 17.7 mA to 15.6 mA at the sensitivity limit. The sensitivity is typically reduced to -102 dBm
Saturation		–16		dBm	`FIFOTHR.CLOSE_IN_RX=0`. See more in DN010 [11]
Adjacent channel rejection -200 kHz offset +200 kHz offset		 12 25		 dB dB	Desired channel 3 dB above the sensitivity limit. 200 kHz channel spacing See Figure 3 for blocking performance at other offset frequencies
Image channel rejection		23		dB	IF frequency 152 kHz Desired channel 3 dB above the sensitivity limit
Blocking ±2 MHz offset ±10 MHz offset		 -50 -40		 dBm dBm	Desired channel 3 dB above the sensitivity limit See Figure 3 for blocking performance at other offset frequencies
250 kBaud data rate, sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (GFSK, 1% packet error rate, 20 bytes packet length, 127 kHz deviation, 540 kHz digital channel filter bandwidth)					
Receiver sensitivity		–95		dBm	Sensitivity can be traded for current consumption by setting `MDMCFG2.DEM_DCFILT_OFF=1`. The typical current consumption is then reduced from 18.9 mA to 16.9 mA at the sensitivity limit. The sensitivity is typically reduced to -91 dBm
Saturation		–17		dBm	`FIFOTHR.CLOSE_IN_RX=0`. See more in DN010 [11]
Adjacent channel rejection		25		dB	Desired channel 3 dB above the sensitivity limit. 750 kHz channel spacing See Figure 4 for blocking performance at other offset frequencies
Image channel rejection		14		dB	IF frequency 304 kHz Desired channel 3 dB above the sensitivity limit
Blocking ±2 MHz offset ±10 MHz offset		 -50 -40		 dBm dBm	Desired channel 3 dB above the sensitivity limit See Figure 4 for blocking performance at other offset frequencies
500 kBaud data rate, sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (MSK, 1% packet error rate, 20 bytes packet length, 812 kHz digital channel filter bandwidth)					
Receiver sensitivity		–90		dBm	`MDMCFG2.DEM_DCFILT_OFF=1` cannot be used for data rates > 250 kBaud
Image channel rejection		1		dB	IF frequency 355 kHz Desired channel 3 dB above the sensitivity limit
Blocking ±2 MHz offset ±10 MHz offset		 -50 -40		 dBm dBm	Desired channel 3 dB above the sensitivity limit See Figure 5 for blocking performance at other offset frequencies
4-FSK, 125 kBaud data rate (250 kbps), sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (1% packet error rate, 20 bytes packet length, 127 kHz deviation, 406 kHz digital channel filter bandwidth)					
Receiver sensitivity		-96		dBm	
4-FSK, 250 kBaud data rate (500 kbps), sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (1% packet error rate, 20 bytes packet length, 254 kHz deviation, 812 kHz digital channel filter bandwidth)					
Receiver sensitivity		-91		dBm	
4-FSK, 300 kBaud data rate (600 kbps), sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (1% packet error rate, 20 bytes packet length, 228 kHz deviation, 812 kHz digital channel filter bandwidth)					
Receiver sensitivity		-89		dBm	

Table 7: RF Receive Section

	Supply Voltage VDD = 1.8 V			Supply Voltage VDD = 3.0 V			Supply Voltage VDD = 3.6 V		
Temperature [°C]	-40	25	85	-40	25	85	-40	25	85
Sensitivity [dBm] 1.2 kBaud	-113	-112	-110	-113	-112	-110	-113	-112	-110
Sensitivity [dBm] 38.4 kBaud	-105	-104	-102	-105	-104	-102	-105	-104	-102
Sensitivity [dBm] 250 kBaud	-97	-96	-92	-97	-95	-92	-97	-94	-92
Sensitivity [dBm] 500 kBaud	-91	-90	-86	-91	-90	-86	-91	-90	-86

Table 8: Typical Sensitivity over Temperature and Supply Voltage, 868 MHz, Sensitivity Optimized Setting

	Supply Voltage VDD = 1.8 V			Supply Voltage VDD = 3.0 V			Supply Voltage VDD = 3.6 V		
Temperature [°C]	-40	25	85	-40	25	85	-40	25	85
Sensitivity [dBm] 1.2 kBaud	-113	-112	-110	-113	-112	-110	-113	-112	-110
Sensitivity [dBm] 38.4 kBaud	-105	-104	-102	-104	-104	-102	-105	-104	-102
Sensitivity [dBm] 250 kBaud	-97	-94	-92	-97	-95	-92	-97	-95	-92
Sensitivity [dBm] 500 kBaud	-91	-89	-86	-91	-90	-86	-91	-89	-86

Table 9: Typical Sensitivity over Temperature and Supply Voltage, 915 MHz, Sensitivity Optimized Setting

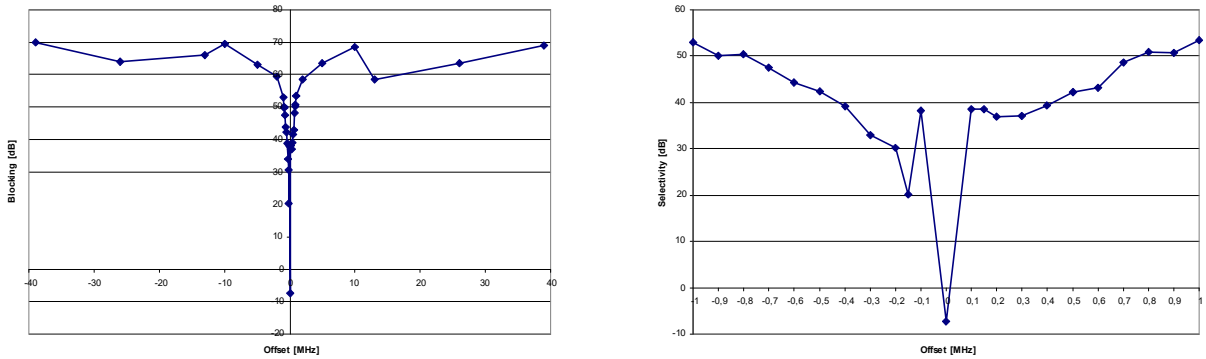


Figure 2: Typical Selectivity at 1.2 kBaud Data Rate, 868.3 MHz, GFSK, 5.2 kHz Deviation. IF Frequency is 152.3 kHz and the Digital Channel Filter Bandwidth is 58 k

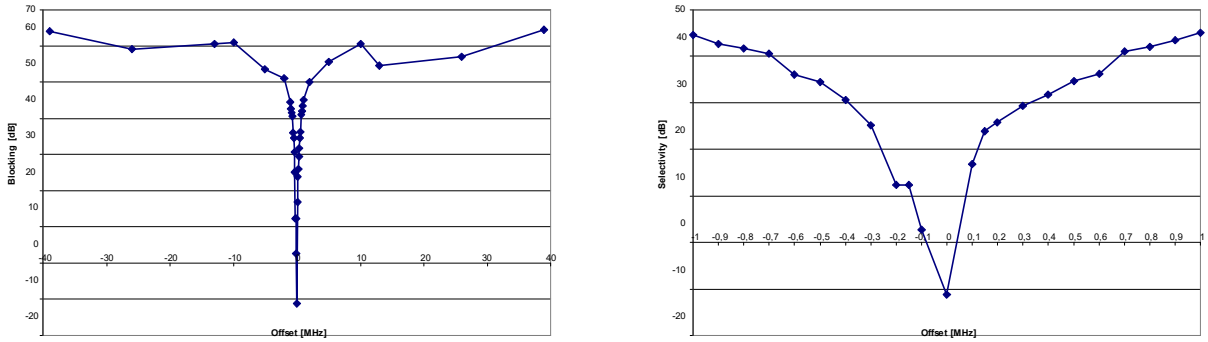


Figure 3: Typical Selectivity at 38.4 kBaud Data Rate, 868 MHz, GFSK, 20 kHz Deviation. IF Frequency is 152.3 kHz and the Digital Channel Filter Bandwidth is 100 kHz

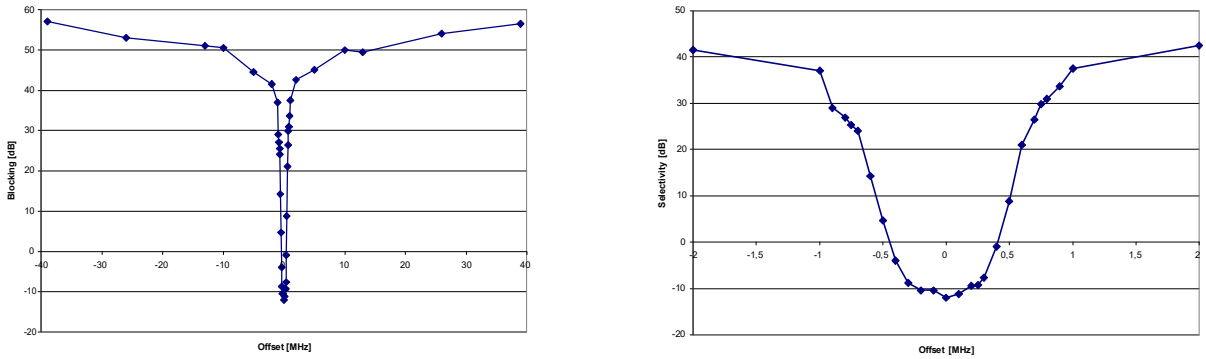


Figure 4: Typical Selectivity at 250 kBaud Data Rate, 868 MHz, GFSK, IF Frequency is 304 kHz and the Digital Channel Filter Bandwidth is 540 kHz

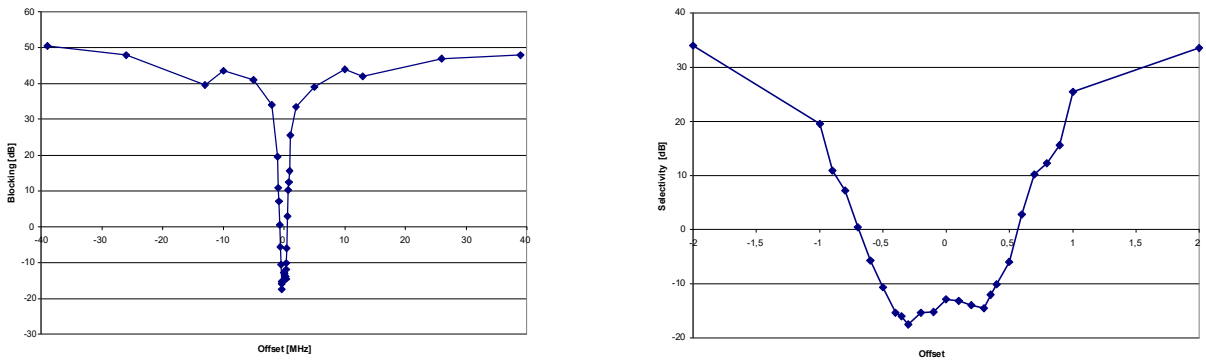


Figure 5: Typical Selectivity at 500 kBaud Data Rate, 868 MHz, GFSK, IF Frequency is 355 kHz and the Digital Channel Filter Bandwidth is 812 kHz

8.3 RF Transmit Section

T_A = 25°C, VDD = 3.0 V, +10 dBm if nothing else stated. All measurement results are obtained using the CC113EM reference designs ([2] and [3]).

Parameter	Min	Typ	Max	Unit	Condition/Note
Differential load impedance					Differential impedance as seen from the RF-port (RF_P and RF_N) towards the antenna. Follow the CC113EM reference designs ([2] and [3]) available from the TI website
315 MHz		122 + j31		Ω	
433 MHz		116 + j41		Ω	
868/915 MHz		86.5 + j43		Ω	
Output power, highest setting					Output power is programmable, and full range is available in all frequency bands. Output power may be restricted by regulatory limits. See also Application Note AN050 [6] and Design Note DN013 [18], which gives the output power and harmonics when using *multi-layer* inductors. The output power is then typically +10 dBm when operating at 868/915 MHz.
315 MHz		+10		dBm	
433 MHz		+10		dBm	
868 MHz		+12		dBm	Delivered to a 50 Ω single-ended load via CC113EM reference designs ([2] and [3]) RF matching network
915 MHz		+11		dBm	
Output power, lowest setting		-30		dBm	Output power is programmable, and full range is available in all frequency bands Delivered to a 50Ω single-ended load via CC113EM reference designs ([2] and [3]) RF matching network
Harmonics, radiated					Measured on CC113EM reference designs ([2] and [3]) with CW, maximum output power
2nd Harm, 433 MHz		-49		dBm	The antennas used during the radiated measurements (SMAFF-433 from R.W. Badland and Nearson S331 868/915) play a part in attenuating the harmonics
3rd Harm, 433 MHz		-40		dBm	
2nd Harm, 868 MHz		-47		dBm	
3rd Harm, 868 MHz		-55		dBm	
2nd Harm, 915 MHz		-50		dBm	Note: All harmonics are below -41.2 dBm when operating in the 902 – 928 MHz band
3rd Harm, 915 MHz		-54		dBm	
Harmonics, conducted					Measured with +10 dBm CW at 315 MHz and 433 MHz
315 MHz		< -35		dBm	Frequencies below 960 MHz
		< -53		dBm	Frequencies above 960 MHz
433 MHz		-43		dBm	Frequencies below 1 GHz
		< -45		dBm	Frequencies above 1 GHz
868 MHz 2nd Harm		-36		dBm	Measured with +12 dBm CW at 868 MHz
other harmonics		< -46		dBm	
915 MHz 2nd Harm		-34		dBm	Measured with +11 dBm CW at 915 MHz (requirement is -20 dBc under FCC 15.247)
other harmonics		< -50		dBm	

Parameter	Min	Typ	Max	Unit	Condition/Note
Spurious emissions conducted, harmonics not included					
					Measured with +10 dBm CW at 315 MHz and 433 MHz
315 MHz		< -58 < -53		dBm dBm	Frequencies below 960 MHz Frequencies above 960 MHz
433 MHz		< -50 < -54 < -56		dBm dBm dBm	Frequencies below 1 GHz Frequencies above 1 GHz Frequencies within 47-74, 87.5-118, 174-230, 470-862 MHz
					Measured with +12 dBm CW at 868 MHz
868 MHz		< -50 < -52 < -53		dBm dBm dBm	Frequencies below 1 GHz Frequencies above 1 GHz Frequencies within 47-74, 87.5-118, 174-230, 470-862 MHz
					All radiated spurious emissions are within the limits of ETSI. The peak conducted spurious emission is -53 dBm at 699 MHz (868 MHz – 169 MHz), which is in a frequency band limited to -54 dBm by EN 300 220. An alternative filter can be used to reduce the emission at 699 MHz below -54 dBm, for conducted measurements, and is shown in Figure 1. See more information in DN017 [12].
					For compliance with modulation bandwidth requirements under EN 300 220 in the 863 to 870 MHz frequency range it is recommended to use a 26 MHz crystal for frequencies below 869 MHz and a 27 MHz crystal for frequencies above 869 MHz. For more information see Application Note AN050 [6].
					Measured with +11 dBm CW at 915 MHz
915 MHz		< -51 < -54		dBm dBm	Frequencies below 960 MHz Frequencies above 960 MHz
TX latency		8		bit	Serial operation. Time from sampling the data on the transmitter data input pin until it is observed on the RF output ports

Table 10: RF Transmit Section

	Supply Voltage VDD = 1.8 V			Supply Voltage VDD = 3.0 V			Supply Voltage VDD = 3.6 V		
Temperature [°C]	-40	25	85	-40	25	85	-40	25	85
Output Power [dBm], PATABLE=0xC0, +12 dBm	12	11	10	12	12	11	12	12	11
Output Power [dBm], PATABLE=0xC5, +10 dBm	11	10	9	11	10	10	11	10	10
Output Power [dBm], PATABLE=0x50, 0 dBm	1	0	-1	2	1	0	2	1	0

Table 11: Typical Variation in Output Power over Temperature and Supply Voltage, 868 MHz

	Supply Voltage VDD = 1.8 V			Supply Voltage VDD = 3.0 V			Supply Voltage VDD = 3.6 V		
Temperature [°C]	-40	25	85	-40	25	85	-40	25	85
Output Power [dBm], PATABLE=0xC0, +11 dBm	11	10	10	12	11	11	12	11	11
Output Power [dBm], PATABLE=0x8E, +0 dBm	2	1	0	2	1	0	2	1	0

Table 12: Typical Variation in Output Power over Temperature and Supply Voltage, 915 MHz

8.4 Crystal Oscillator

T_A = 25°C, VDD = 3.0 V if nothing else is stated. All measurement results obtained using the CC113EM reference designs ([2] and [3]).

Parameter	Min	Typ	Max	Unit	Condition/Note
Crystal frequency	26	26	27	MHz	For compliance with modulation bandwidth requirements under EN 300 220 in the 863 to 870 MHz frequency range it is recommended to use a 26 MHz crystal for frequencies below 869 MHz and a 27 MHz crystal for frequencies above 869 MHz. For more information see Application Note AN050 [6].
Tolerance		±40		ppm	This is the total tolerance including a) initial tolerance, b) crystal loading, c) aging, and d) temperature dependence. The acceptable crystal tolerance depends on RF frequency and channel spacing / bandwidth.
Load capacitance	10	13	20	pF	Simulated over operating conditions
ESR			100	Ω	
Start-up time		150		µs	This parameter is to a large degree crystal dependent. Measured on the CC113EM reference designs ([2] and [3]) using crystal AT-41CD2 from NDK

Table 13: Crystal Oscillator Parameters

8.5 Low Power RC Oscillator

T_A = 25°C, VDD = 3.0 V if nothing else is stated. All measurement results obtained using the CC113EM reference designs ([2] and [3]).

Parameter	Min	Typ	Max	Unit	Condition/Note
Calibrated frequency	34.7	34.7	36	kHz	Calibrated RC Oscillator frequency is XTAL frequency divided by 750
Frequency accuracy after calibration			±1	%	
Temperature coefficient		+0.5		% / °C	Frequency drift when temperature changes after calibration
Supply voltage coefficient		+3		% / V	Frequency drift when supply voltage changes after calibration
Initial calibration time		2		ms	When the RC Oscillator is enabled, calibration is continuously done in the background as long as the crystal oscillator is running

Table 14: RC Oscillator Parameters

8.6 Frequency Synthesizer Characteristics

T_A = 25°C, VDD = 3.0 V if nothing else is stated. All measurement results are obtained using the CC113EM reference designs ([2] and [3]). Min figures are given using a 27 MHz crystal. Typ and max figures are given using a 26 MHz crystal.

Parameter	Min	Typ	Max	Unit	Condition/Note
Programmed frequency resolution	397	$F_{XOSC}/2^{16}$	412	Hz	26-27 MHz crystal. The resolution (in Hz) is equal for all frequency bands
Synthesizer frequency tolerance		±40		ppm	Given by crystal used. Required accuracy (including temperature and aging) depends on frequency band and channel bandwidth / spacing
RF carrier phase noise		–92		dBc/Hz	@ 50 kHz offset from carrier
RF carrier phase noise		–92		dBc/Hz	@ 100 kHz offset from carrier
RF carrier phase noise		–92		dBc/Hz	@ 200 kHz offset from carrier
RF carrier phase noise		–98		dBc/Hz	@ 500 kHz offset from carrier
RF carrier phase noise		–107		dBc/Hz	@ 1 MHz offset from carrier
RF carrier phase noise		–113		dBc/Hz	@ 2 MHz offset from carrier
RF carrier phase noise		–119		dBc/Hz	@ 5 MHz offset from carrier
RF carrier phase noise		–129		dBc/Hz	@ 10 MHz offset from carrier
PLL turn-on / hop time	85.1	88.4	88.4	µs	Time from leaving the IDLE state until arriving in the RX, FSTXON or TX state, when not performing calibration. Crystal oscillator running
PLL RX/TX settling time	9.3	9.6	9.6	µs	Settling time for the 1·IF frequency step from RX to TX
PLL TX/RX settling time	20.7	21.5	21.5	µs	Settling time for the 1·IF frequency step from TX to RX
PLL calibration time	694	721	721	µs	Calibration can be initiated manually or automatically before entering or after leaving RX/TX

Table 15: Frequency Synthesizer Parameters

8.7 Analog Temperature Sensor

T_A = 25°C, VDD = 3.0 V if nothing else is stated. All measurement results obtained using the CC113EM reference designs ([2] and [3]). Note that it is necessary to write 0xBF to the `PTEST` register to use the analog temperature sensor in the IDLE state.

Parameter	Min	Typ	Max	Unit	Condition/Note
Output voltage at –40°C		0.651		V	
Output voltage at 0°C		0.747		V	
Output voltage at +40°C		0.847		V	
Output voltage at +80°C		0.945		V	
Temperature coefficient		2.47		mV/°C	Fitted from –20 °C to +80 °C
Error in calculated temperature, calibrated	-2 *	0	2 *	°C	From –20 °C to +80 °C when using 2.47 mV / °C, after 1-point calibration at room temperature * The indicated minimum and maximum error with 1-point calibration is based on simulated values for typical process parameters
Current consumption increase when enabled		0.3		mA	

Table 16: Analog Temperature Sensor Parameters

8.8 DC Characteristics

T_A = 25°C if nothing else stated.

Digital Inputs/Outputs	Min	Max	Unit	Condition
Logic "0" input voltage	0	0.7	V	
Logic "1" input voltage	VDD-0.7	VDD	V	
Logic "0" output voltage	0	0.5	V	For up to 4 mA output current
Logic "1" output voltage	VDD-0.3	VDD	V	For up to 4 mA output current
Logic "0" input current	N/A	–50	nA	Input equals 0V
Logic "1" input current	N/A	50	nA	Input equals VDD

Table 17: DC Characteristics

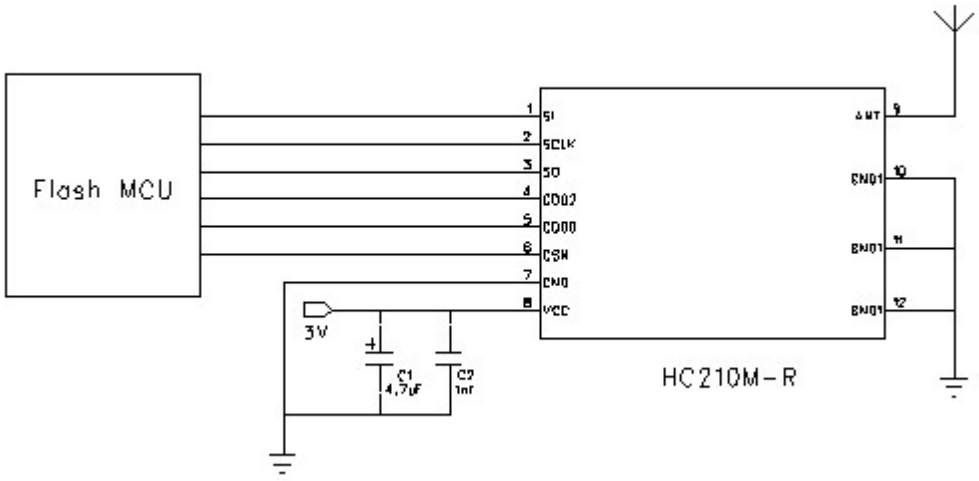
8.9 Power-On Reset

For proper Power-On-Reset functionality the power supply should comply with the requirements in Table 18 below. Otherwise, the chip should be assumed to have unknown state until transmitting an `SRES` strobe over the SPI interface. See Section on page 48 for further details.

Parameter	Min	Typ	Max	Unit	Condition/Note
Power-up ramp-up time			5	ms	From 0V until reaching 1.8V
Power off time	1			ms	Minimum time between power-on and power-off

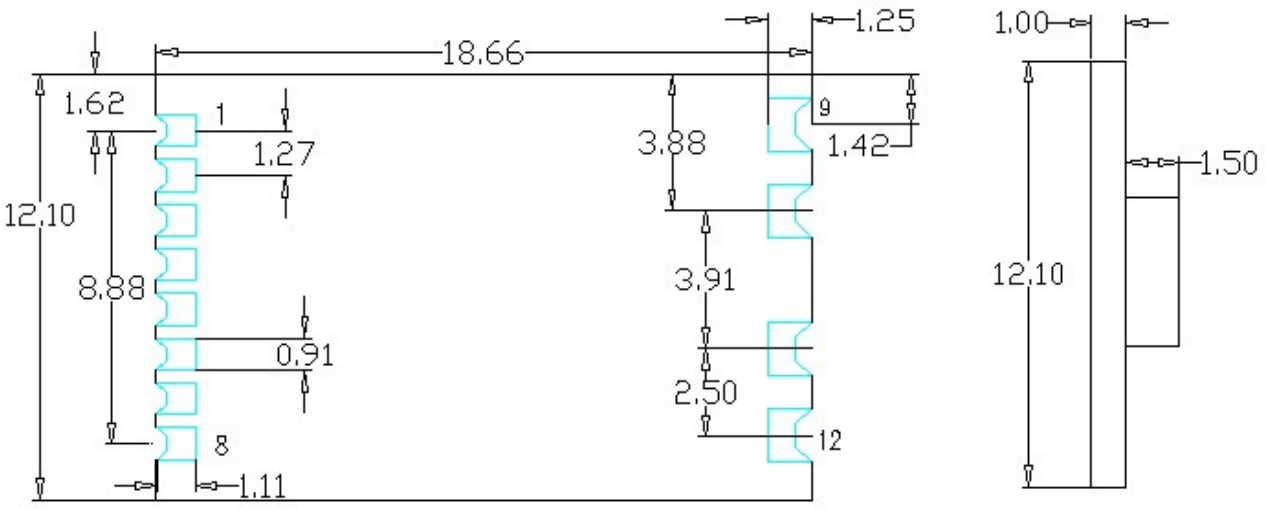
Table 18: Power-On Reset Requirements

9. Appication



10. Module Package Outline Drawing

Unit: mm



11. Ordering Information

Part Number	Operation Band
HC210M-R 315	315MHz
HC210M-R 433	433MHz
HC210M-R 868	868MHz
HC210M-R 915	915MHz

12. Module Revisions

Revisions	Date	Updated History
Rev1.0	April 2017	The first final release

13. Importance Notice

The HC210M-R datasheet will be changed by LJ ELECTRONICS TECHNOLOGY LIMITED according to the module design.

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